Further Analysis of a Sigma–Delta Resistance-to-Digital Converter for Differential Resistive Sensors

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***Abstract* – We analyze the proposed Sigma–Delta Resistance-to-Digital Converter for Differential Resistive Sensors further for relative error contributed by the number of samples and that due to small variations in differential resistive sensors. We believe that it is an extension of the error analysis part of what is already reported in [1], and hence is worth reporting. Using analysis similar to the original paper and computer simulation, we develop a maximal value of relative error that is not contributed by the hardware, but it is contributed by limitations of the proposed method. Such error is inversely proportional both to the changes in differential resistors and to the number of samples that are being averaged.**

I. INTRODUCTION

Analog-to-digital converter (ADC) is an important piece of instrumentation used as a component or as part of an integrated microcontroller meant for making measurements. There are many types of ADCs, and each type has its advantages and disadvantages. The Sigma-Delta ADC is quite accurate and popular but somewhat slower than conventional ADCs. It is interesting that this ADC is using only 1-bit quantizer (2 level midriser) can achieve same accuracy as converters with more quantization levels [3].

Differential resistive sensors can be used for the measurement of physical quantities such as displacement and pressure. This sensor can be modeled as two resistors connected in one common terminal and the value of the first resistor (R1) is increasing linearly with the physical quantity while second resistor (R2) is decreasing linearly [1].

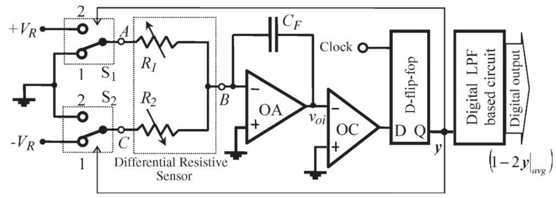

Fig. 1 Sigma-delta resistance-to-digital converter

Novel approach of converting a signal from differential resistive sensor directly to digital signal is proposed [1]. In Section II of this paper we will briefly describe operation of this circuit, for the complete description please refer to the original paper. Paper of the proposal is discussing effects of hardware imperfections, such as stray resistance and capacitance values, mismatch in reference voltages, limitations of OP AMPs used, etc. In the Section III of this paper we focus on reading errors that are contributed by the limited number of samples in the averaging process. Moreover, percentage of change of resistance in sensors may contribute to the error when such relative change is not large enough. These fact derived from the theory are simulated afterwards using a computer, results of the simulation are described in Section IV.

II. CIRCUIT ANALYSIS

Proposed Sigma-Delta Resistance-to-Digital converter for differential resistive sensors [1] is shown in Figure 1. Value of voltage v_{oi}, the output of integrator, is the focus of analysis. For

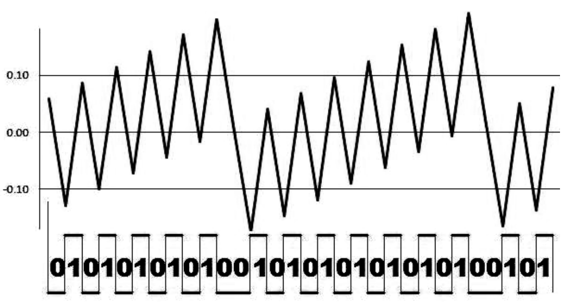

Fig. 2 Voltage v_{oi} and digital output y over time

$y=1$, v_{oi} is going to ramp-up by voltage $V_R T_C/(R_2 C_F)$, and for $y=0$, v_{oi} is going to ramp-down by voltage $-V_R T_C/(R_1 C_F)$, where T_C is period between samples. An example of voltage v_{oi} over time is shown in Figure 2. Considering voltage v_{oi} only at the times of sampling, when this voltage is close to 0 volts, it is expected that maximum or minimum value of voltage v_{oi} are attained at the next sampling. Assuming that voltage v_{oi} is just below 0 volts and ramp-up will occur during the next sampling period, at the next sampling we expect voltage to be $v_{oi}=V_R T_C/(R_2 C_F)$. This is maximum attainable voltage, since for positive values of v_{oi} it is going to ramp-down at the next sampling. Similarly, for voltage just above 0 volts it is going to ramp-down, and minimum achievable voltage of v_{oi} is $-V_R T_C/(R_1 C_F)$. Voltage lower than this minimum cannot be achieved, because assuming that voltage is negative for the current sampling, until the next sampling voltage will ramp-up and increase. Combining these results we get following bounds

$$\frac{-V_R T_C}{R_1 C_F} \le v_{oi} \le \frac{V_R T_C}{R_2 C_F} \qquad (1)$$

In some cases voltage v_{oi} follows a simple pattern, and these bounds are not tight, however most of the time voltage v_{oi} displays chaotic behavior and these bounds are attainable. Meaning that, there is non-zero probability that voltage v_{oi} can be found on any regular interval inside these bounds.

Output y is observed over time T, and N samples are collected ($T=NT_C$). Let $N_{(0)}$ and $N_{(1)}$ be counts on number of times digital output y was 0 and 1, respectively ($N=N_{(0)}+N_{(1)}$). Assuming that integrator output is initially zero, integrator output [1] is

$$v_{oi}=N_{(1)}\frac{V_R T_C}{R_2 C_F}-N_{(0)}\frac{-V_R T_C}{R_1 C_F} \qquad (2)$$

Applying bounds (1) on equation (2), and multiplying by $C_F R_1 R_2/(V_R T_C)$ we arrive at

$$-R_2 \le N_{(1)}R_1 - N_{(0)}R_2 \le R_1$$

Differential resistors have property $R_1=R_0(1+kx)$ and $R_2=R_0(1-kx)$, substituting these values of resistors and diving by R_0

$$-(1-kx)\le N_{(1)}(1+kx)-N_{(0)}(1-kx)\le(1+kx)$$

Subtracting left side

$$0\le N_{(1)}(1+kx)-N_{(0)}(1-kx)+1-kx\le 2$$

Substituting $N_{(0)}=N-N_{(1)}$

$$0\le(N-1)(kx-1)+2N_{(1)}\le 2$$

Subtracting $2N_{(1)}$ and dividing by $(N-1)$

$$\frac{-2N_{(1)}}{N-1}\le(kx-1)\le\frac{2-2N_{(1)}}{N-1}$$

Finally, by adding one we get the range of kx

$$1-2\frac{N_{(1)}}{N-1}\le kx\le 1-2\frac{N_{(1)}-1}{N-1} \qquad (3)$$

Assuming that $N_{(1)}$ is large compared to integer 1, this simplifies to an approximation of kx

$$kx=1-2\left(\frac{N_{(1)}}{N}\right)=1-2y\big|_{avg} \qquad (4)$$

III. Relative error of $1-2y\big|_{avg}$

Expression (3) shows that measured value of kx may have errors which are not contributed by hardware, instead they result from averaging limited number of samples. Computing difference between upper and lower bound of kx gives us maximal absolute error

$$\left(1-2\frac{N_{(1)}-1}{N-1}\right)-\left(1-2\frac{N_{(1)}}{N-1}\right)=\frac{2}{N-1}$$

Moreover, dividing absolute error by value of kx will result in maximum of relative error

$$\frac{2}{(N-1)kx}$$

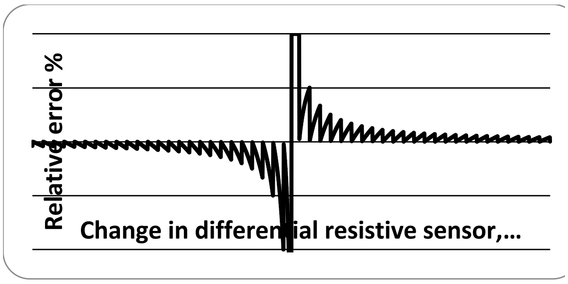

Fig. 3 Relative error for $N = 500$

In the next section by using a simulation we will show that this error does show as predicted by theory.

IV. SIMULATION

Excel can be used as a simulation tool for Sigma–Delta converters [2]. Rows are used to represent discrete time, and columns to denote quantities being simulated. Excel correctly simulates Sigma–Delta converters using discrete time steps. Furthermore, analysis of results can be done in Excel, for instance noise shaping property of converters can be confirmed [2]. In this research, Excel spreadsheet was converted into a C++ program. This program is using the same algorithm, only difference is that it can simulate faster, and it can show the results as a variation of parameters N and kx. It would be possible to do this using Excel as well, however it would be much more complicated.

Figure 3 shows relative error in simulation for fixed number of samples and varying kx from -0.1 to 0.1. As theory of the previous section suggests, relative error is inversely proportional to change in differential resistance kx. Figure 4 shows relative errors from simulation of fixed kx and varying N. As number of samples is larger, relative error drops as a result of being inversely proportional to N. Note that this simulation of the circuit does not include any hardware error simulation, therefore all errors are result of the imperfection stemming from the method itself.

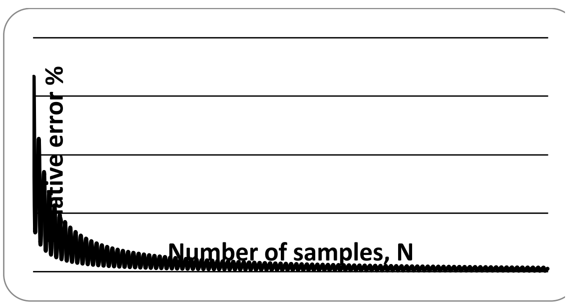

Fig. 4 Relative error for $kx = 0.3$

V. CONCLUSION

Considering an input signal of sensor that is rapidly changing in time, Sigma-Delta conversion requires oversampling of input signal, which in turn will need a clock of a faster rate, thus enabling it to deliver high number of samples. Large samples per unit time, implies higher frequency of the clock and faster processing hardware. In this paper, by analysis and simulation of the circuit, we have confirmed that relative error of measured quantity increases beyond tolerable level for large values of $(Nkx)^{-1}$. For the purpose of Micro-Electro-Mechanical Systems (MEMS) implementation, integrated hardware has operating frequency limitations [3].

Error analysis presented here is useful if output stream is computed by counting number of ones over fixed number of samples. This is not directly applicable to [1] since this design includes a digital low-pass filter instead of a counting method assumed here. Without this low-pass filter, the noise shaping abilities of sigma-delta modulator are not exploited [4], and consequently out-of-band quantization noise is present. This only further shows the importance of digital filters over the conventional methods.

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